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Hon'ble Vice-Chancellor, MPUAT, Udaipur

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Dr. Deepak Sharma, Administrative Officer, CTAE
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Mr. Lalit Verma, ECE Deparment, CTAE
Mr. Neeraj Chaoudhary, ECE Deparment, CTAE

Workshop
on
VLSI Design and Testing Using EDA Tools
(March 18, 2019)

REGISTRATION FORM

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(In block letters)

Institution _____

Address _____
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Date _____ Signature _____

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Department of
Electronics and Communication Engineering

College of Technology and Engineering,
MPUAT, Udaipur

&

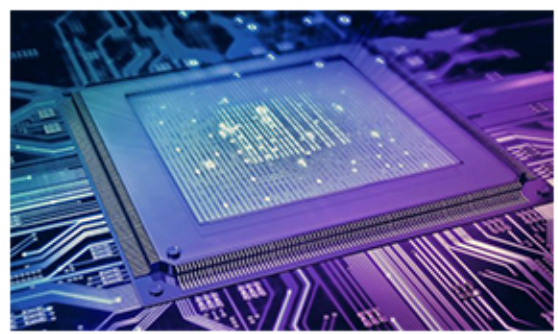
Malaviya National Institute of Technology
Jaipur

Jointly organizes

One day Workshop on

VLSI Design and Testing using EDA Tools

March 18, 2019



TECHNICAL EDUCATION QUALITY IMPROVEMENT PROGRAMME-III

Venue
Department of Electronics and Communication Engineering,
CTAE, MPUAT Udaipur-313001

ABOUT WORKSHOP

The objective of the workshop is to impart knowledge about technologies and trends pertaining to EDA tools in VLSI. Recent breakthrough in the silicon photonic technology are enabling the integration of optical devices into silicon based semiconductor processes. This is motivating investigations into applications beyond the traditional telecom. The workshop will be useful in updating domain knowledge and expertise.

LEARNINGS

Understanding the design automation for integrated optic system.

Understanding the EDA inspired design flow and synthesis for optical design automation.

Learning CAD for the design and the fabrication of optical logic chip.

Understanding the opportunities in the area of design automation.

Knowing about VLSI EDA tools.

AREAS TO BE COVERED IN THE WORKSHOP

SESSION I

Presenting work on design automation for integrated optic system, building block model for optical devices, EDA inspired design flow & synthesis algorithms for optical design automation, Boolean function decomposition, technology mapping, interconnect routing, thermal aware synthesis, research chaleges and opportunitis in the area of design automtion for hybrid integration of Si photonics and CMOS technologies.

SESSION II

Back End Design in IC Nanometer Design, Custom IC Design (Back End), Need for ASIC, introduction to Mentor Graphics design flow, TANNER, Schematic design –Tanner EDA Tool, Functional Simulation (T-Spice), Waveform Viewer (W-Edit), Layout design (L-Edit), Physical verification with Mentor Graphics Calibre Tool, DRC, LVS, PEX, PERC, FPGA Design Flow, HDL Designer, ASIC Design using Leonardo Spectrum Tool, FPGA using Mentor Graphics Precision Synthesis Tool.

SPEAKERS

Dr. Priyank Kalla
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Department of Electrical & Computer Engineering, University of Utah,
Salt Lake City, USA

Mr. Upendra Kumar Gupta
Application Engineer
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